IN THE CLAIMS

Please amend the claims as follows:

Listing of Claims:

Claims 1-18 (Canceled).

19. (New) A programmable logic circuit comprising:

a plurality of unit logic circuits connected in parallel;

an input signal control section that supplies input signals received from outside to the plurality of unit logic circuits; and

an output signal control section that supplies output signals of the plurality of unit logic circuits to outside,

each of the plurality of unit logic circuits comprising:

a logic operation section that performs predetermined logic operation on the input signals and generates data, said logic operation section having functions that are changeable based on first setting information;

a data processing section that generates data by carrying out arrangement, duplication and inversion processing on the data from the logic operation section based on second setting information, and provides the data to the output signal control section as output signals;

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a storage section that stores the first and second setting information; and

a memory control section that takes control by receiving jump setting information, reading out either the first or the second setting information of the storage section based on the jump setting information and providing the setting information to the logic operation circuit and the data processing section,

wherein each of the plurality of unit logic circuits sequentially changes some or all of the functions of the logic operation section and the data processing section based on the first and second setting information read out sequentially from the storage section and carries out predetermined operations of a sequential circuit.

20. (New) A programmable logic circuit comprising:

a plurality of unit logic circuits connected in parallel;

an input signal control section that supplies input signals received from outside to the plurality of unit logic circuits; and

an output signal control section that supplies output signals of the plurality of unit logic circuits to outside,

each of the plurality of unit logic circuits comprising:

a logic operation section that performs predetermined logic operation on the input signal and generates data, said logic operation section having functions that are changeable based on first setting information;

a data processing section that generates data by carrying out arrangement, duplication and inversion processing on the data from the logic operation section based on the second setting information, and provides the data to the output signal control section as output signals;

a storage section that stores the first and second setting information; and

a memory control section that receives stopping setting information and controls stopping between the logic operation section and the data processing section based on the stopping setting information,

wherein each of the plurality of unit logic circuits sequentially changes some or all of the functions of the logic operation section and the data processing section based on the first and second setting information read out sequentially from the storage section and carries out predetermined operations of a sequential circuit.

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21. (New) The programmable logic circuit according to claim 19, wherein the logic operation section further comprises a logic cell that performs predetermined logic operation on the input signals and generates data, said logic cell having functions that are changeable based on the first setting information.

22. (New) The programmable logic circuit according to claim 20, wherein the logic operation section further comprises a logic cell that performs predetermined logic operation on the input signals and generates data, said logic cell having functions that are changeable based on the first setting information.

23. (New) The programmable logic circuit according to claim 19, wherein the data processing section further comprises a cross-connecting switch that generates data by carrying out arrangement, duplication and inversion processing on the data from the logic operation section based on the second setting information.

24. (New) The programmable logic circuit according to claim 20, wherein the data processing section further comprises a cross-connecting switch that generates data by carrying out

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arrangement, duplication and inversion processing on the data from the logic operation section based on the second setting information.

25. (New) The programmable logic circuit according to claim 23, wherein the data processing section comprises a flip-flop that holds the data from the cross-connecting switch and supplies the data to the output signal control section as the output signals.

26. (New) The programmable logic circuit according to claim 24, wherein the data processing section comprises a flip-flop that holds the data from the cross-connecting switch and supplies the data to the output signal control section as the output signals.

27. The programmable logic circuit according to claim 19, further comprising a connecting section that connects one unit logic circuit in the plurality of unit logic circuits and another unit logic circuit neighboring the one unit logic circuit in physical arrangement,

wherein the logic operation section performs predetermined logic operation on one of the input signal and data from the another neighboring unit logic circuit and generates data, said logic operation section having functions that are changeable based on first setting information.

28. (New) The programmable logic circuit according to claim 20, further comprising a connecting section that connects one unit logic circuit in the plurality of unit logic circuits and another unit logic circuit neighboring the one unit logic circuit in physical arrangement,

wherein the logic operation section performs predetermined logic operation on one of the input signal and data from the another neighboring unit logic circuit and generates data, said logic operation section having functions that are changeable based on first setting information.

29. (New) The programmable logic circuit according to claim 28, wherein the logic operation section further comprises a logic cell that performs predetermined logic operation on the input signals and generates data, said logic cell having functions that are changeable based on the first setting information.

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30. (New) The programmable logic circuit according to claim 23, wherein the data processing section comprises a flip-flop that holds the data from the cross-connecting switch and supplies the data to the output signal control section as the output signals.

31. (New) The programmable logic circuit according to claim 24, wherein the data processing section comprises a flip-flop that holds the data from the cross-connecting switch and supplies the data to the output signal control section as the output signals.

32. A programmable logic circuit comprising:

a plurality of unit logic circuits connected in parallel;

an input signal control section that supplies input signals received from outside to the plurality of unit logic circuits; and

an output signal control section that supplies output signals of the plurality of unit logic circuits to outside, the input signal control section comprising:

a section that supplies a control signal to the plurality of unit logic circuits based on the input signal; and

a section that supplies index information to the plurality
of unit logic circuits at the time of receiving an index
designation signal,

each of the plurality of unit logic circuits comprising:

a logic operation section that performs predetermined logic
operation on the input signal and generates data, said logic
operation section having functions that are changeable based on
any of the first setting information;

a data processing section that carries out arrangement,
duplication, and inversion processing on the data from the logic
operation section based on any of the second setting information,
generates data and provides the data to the output signal control
section as the output signals;

a storage section storing the first and second setting
information; and

a memory control section that stores a lead position address
indicating the lead position of storage position addresses of the
first and second setting information at the storage section based
on one of the control signal and index information at the time of
receiving one of the control signal and the index information,

wherein each of the plurality of unit logic circuits
sequentially changes some or all of the functions of the logic

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operation section and the data processing section based on either the first or second setting information read out sequentially from the storage section based on the lead position address stored in the memory control section and carries out predetermined operations of a sequential circuit.

33. (New) The programmable logic circuit according to claim 32, wherein the logic operation section further comprises a logic cell that performs predetermined logic operation on the input signals and generates the data, said logic cell having functions that are changeable based on the first setting information.

34. (New) The programmable logic circuit according to claim 32, wherein the data processing section further comprises a cross-connecting switch that generates data by carrying out arrangement, duplication and inversion processing on the data from the logic operation section based on the second setting information.

35. (New) The programmable logic circuit according to claim 34, wherein the data processing section comprises a flip-flop that holds the data from the cross-connecting switch and supplies

the data to the output signal control section as the output signals.

36.   The programmable logic circuit according to claim 32, further comprising a connecting section that connects one unit logic circuit in the plurality of unit logic circuits and another unit logic circuit neighboring the one unit logic circuit in physical arrangement,

wherein the logic operation section performs predetermined logic operation on one of the input signal and data from the another neighboring unit logic circuit and generates data, said logic operation section having functions that are changeable based on first setting information.